Dynamic Response of Normal and Corbino a-Si:H TFTs for AM-OLEDs

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***Abstract*—The dynamic characteristics of normal and Corbino hydrogenated amorphous silicon (a-Si:H) thin-film transistors (TFTs) have been investigated. Top- and bottom-gate normal a-Si:H TFTs and bottom-gate Corbino a-Si:H TFTs were fabricated with a five-photomask process used in the processing of the active-matrix liquid crystal displays. The charging time and feedthrough voltage ΔV_P measurement indicates that the normal a-Si:H TFT shows a similar behavior regardless of its TFT geometrical structure. Using a simple gate-to-source capacitance $C_{\rm GS}$ model, the dependence of ΔV_P on gate-to-source overlap and storage capacitor has closely been estimated using analytical calculation. Due to a unique electrode geometry, the Corbino a-Si:H TFT shows a small deviation from an analytical model used for the normal a-Si:H TFT, and consequently, a modified analytical model was developed. We also developed concepts of its possible application as a switching device to active-matrix organic light-emitting displays.**

***Index Terms*—AC response, active-matrix organic light-emitting display (AM-OLED), bottom gate, corbino, dynamic measurement, dynamic response, hydrogenate amorphous silicon (a-Si:H), thin-film transistor (TFT), top gate, transient response.**

I. Introduction

TO DATE, the active-matrix organic light-emitting display (AM-OLED) has attracted many interests from both industries and academia due to its superior properties over other flat-panel displays such as light weight, thin thickness, high brightness, high contrast ratio, wide view angle, and deep color saturation. From small-size displays for portable devices to large-size displays for monitors and TV applications, AM-OLEDs are regarded as the next-generation display technology expecting to replace existing flat-panel displays. In particular, due to matured active-matrix liquid crystal display (AM-LCD) manufacturing technology, hydrogenate amorphous silicon (a-Si:H) technology is considered as an ideal candidate for active-matrix arrays (so-called backplane) for the large-size high-resolution AM-OLED. Today, many researchers are trying to develop a more stable backplane pixel electrode circuit with the compensation that can overcome the a-Si:H electrical instability. Because of its inherent low field-effect mobility and large parasitic capacitive elements originated from its relatively simple low-resolution processing steps in comparison to silicon or polysilicon technologies, a-Si:H thin-film transistor (TFT) pixel electrode circuits show different dynamic responses from other well-established technologies. Historically, in 1990s, several research groups [1]–[4] have reported measurement technique and analysis of the dynamic characteristics of a-Si:H TFTs for AM-LCDs. Dawson *et al.* also showed the transient response of the OLED in combination with the polysilicon-based pixel electrode circuits for the AM-OLED [5]. However, so far, the detailed study of the operational condition and the capacitive element effects on the dynamic characteristics of the a-Si:H TFT pixel electrode circuit for the AM-OLED have not been described.

This paper discusses the dynamic characteristics of top- and bottom-gate a-Si:H TFTs that can be used in AM-OLEDs. The device fabrications of top- and bottom-gate a-Si:H TFTs were previously described [6], and the experimental setup used for the dynamic measurement is described in this paper. The charging characteristics of top-gate a-Si:H TFTs are addressed in the second part of this paper. The discussion, in particular, focuses on the effect of storage capacitance and TFT gate-to-source overlap on the switching TFT charging performance. Then, the feedthrough voltage in the AM-OLED pixel electrode circuit and its variation with TFT geometries and driving signal are discussed. Finally, we discuss the dynamic characteristics of bottom-gate a-Si:H Corbino and normal TFTs. We present the feedthrough voltage property of the a-Si:H Corbino TFT [7] in comparison to the normal a-Si:H TFT and simulate the dynamic characteristics based on the top-gate a-Si:H TFT extracted parameters. To our best knowledge, this paper represents the first investigation of the dynamic electrical characteristics of Corbino a-Si:H TFTs and their possible application to AM-OLEDs.

II. a-Si:H TFT Fabrication

A. Top-Gate a-Si:H TFTs

To characterize the dynamic behavior of the a-Si:H TFT (charging and hold performance), top-gate a-Si:H TFTs with various storage capacitors are fabricated (Fig. 1) [6]. For this experiment, an a-Si:H TFT with a channel length of 10 μm and a width of 1000 μm is commonly used for various storage capacitors. The overlap between source/drain (S/D) and gate electrodes (OVL) is maintained as 4 μm. The source electrode of the a-Si:H TFT is connected to a storage capacitor. In

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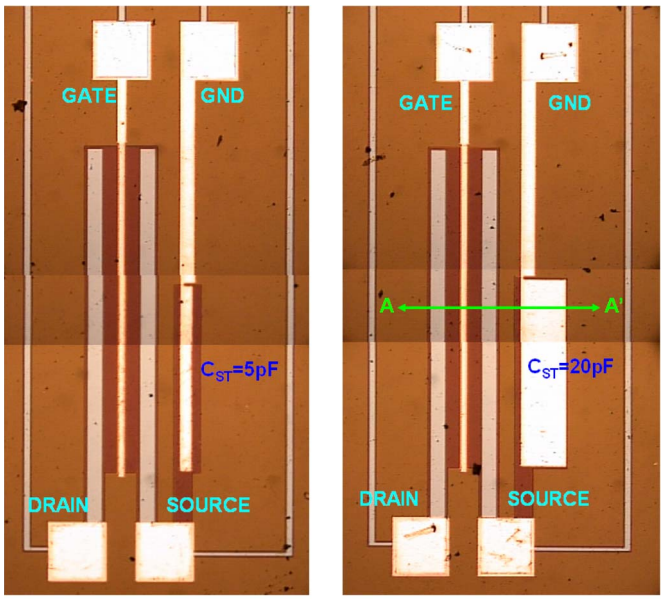

Fig. 1. Top views of top-gate a-Si:H TFTs ($W/L = 1000/10$) with a storage capacitor of (a) 5 pF and (b) 20 pF.

order to minimize the experimental perturbation, the size of the capacitor is set as 5, 10, 20, or 50 pF, which is about 10–100 times larger than that of the actual storage capacitor used in the AM-OLED pixel electrode circuit (~500 fF). Fig. 1 shows the top views of fabricated top-gate a-Si:H TFTs with a storage capacitor. It should be noted that these capacitor values are subject to the insulator thickness, and the designed capacitance values are obtained for a 3300-Å-thick a-SiN_x:H insulator. Four different storage capacitance values were achieved by changing the capacitor area, as shown in Fig. 1.

B. Bottom-Gate a-Si:H TFTs

The bottom-gate Corbino a-Si:H TFTs of different geometries with various storage capacitors have been fabricated to characterize the feedthrough voltage behavior of the Corbino a-Si:H TFT in comparison to the top-gate TFT (Fig. 2). For this experiment, the channel length of the Corbino a-Si:H TFT is fixed at 6 μm, whereas the channel width varies from 88 to 245 μm. The sizes of storage capacitors are also fixed at 0.9 and 2.5 pF, which are close to the actual values of the AM-OLED pixel electrode design. Due to the unique geometry of the Corbino TFT, the overlap between S/D and gate electrodes can be 5, 8, or 10 μm. The source electrode of the a-Si:H TFT is connected to a storage capacitor. For a direct comparison, we also fabricated at the same time the normal rectangular a-Si:H TFTs with the same geometries (same channel length and width) to measure the feedthrough voltage behavior in comparison to Corbino a-Si:H TFTs (Fig. 2). As in Corbino a-Si:H TFTs, the sizes of storage capacitors are fixed at 0.9 and 2.5 pF, and the overlaps between S/D and gate electrodes are fixed at 2.0 μm. Table I summarizes the geometric parameters of different Corbino a-Si:H TFTs and normal rectangular a-Si:H TFTs with various storage capacitors. All bottom-gate

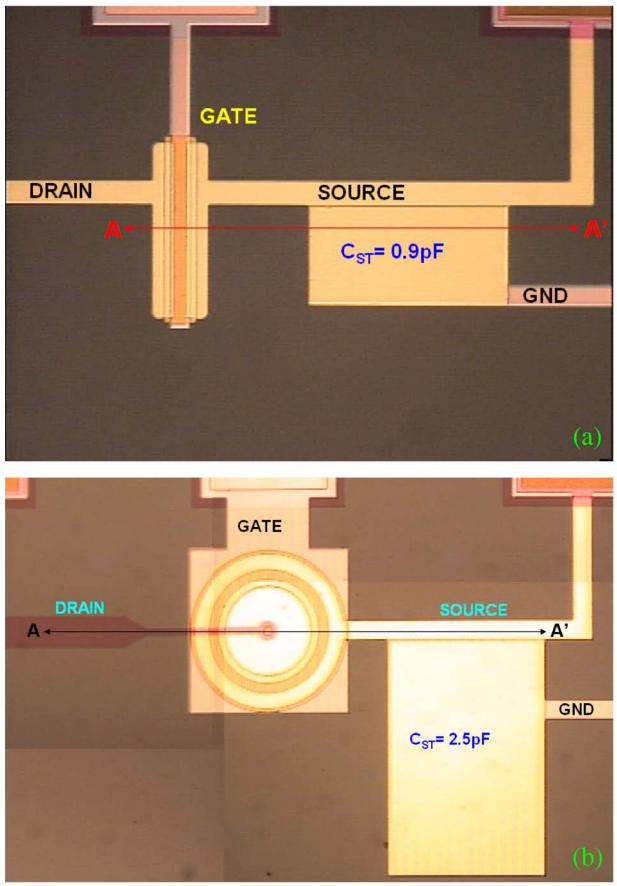

Fig. 2. (a) Top views of normal a-Si:H TFTs with a channel width-over-length ratio of 88/6 and a storage capacitor of 0.9 pF. (b) Top views of Corbino a-Si:H TFTs with a channel width-over-length ratio of 245/6 and a gate-to-source overlap of 8 μm.

a-Si:H TFTs were fabricated using the normal AM-LCD five-photomask process steps [8]. More specifically, on the Corning Eagle 2000 glass substrate, a bilayer of aluminum–neodymium compound (AlNd, 2000 Å) and molybdenum (Mo, 500 Å) was deposited by a sputtering method. The Mo/AlNd gate electrode was then patterned by wet etching (Mask 1). Following gate electrode definition, a hydrogenated amorphous silicon nitride (a-SiN_x:H, 4000 Å)/a-Si:H (1700 Å)/phosphorous-doped a-Si:H (n^+ a-Si:H, 300 Å) trilayer was deposited by plasma-enhanced chemical vapor deposition (PECVD) at 350 °C to form a gate insulator and an active channel layer, respectively. After defining the device active island by reactive-ion etching (RIE; Mask 2), a chromium (Cr, 1200 Å) layer was deposited by sputtering, and S/D electrodes were patterned by wet etching (Mask 3). Using S/D metal and photoresist as masks, back-channel etching by RIE was performed. Then, we deposited a-SiN_x:H (3000 Å) as a passivation layer by PECVD at 300 °C. To make a contact for the pixel electrode indium tin oxide (ITO), a via was formed through the passivation layer by RIE (Mask 4). After contact via definition, ITO (500 Å) was deposited by a sputtering method at room temperature, and then, pixel electrodes were patterned by wet etching (Mask 5). As a final step, device thermal annealing was performed for an hour at 235 °C; this step is needed to improve ITO optical and electrical properties.

TABLE I
GEOMETRIC PARAMETERS OF NORMAL a-Si:H TFTs AND CORBINO a-Si:H TFTs WITH VARIOUS STORAGE CAPACITORS AND GATE-TO-SOURCE OVERLAPS

Normal	Width [μm]	Length [μm]	C_{ST} [pF]	C_{GSO} [pF]	OVL [μm]
(a)	88	6	0.9	0.026	2
(b)	245	6	2.5	0.074	2

				Fabricated		Target	
Corbino	Width [μm]	Length [μm]	C_{ST} [pF]	C_{GSO} [pF]	OVL [μm]	C_{GSO} [pF]	OVL [μm]
(c)	88	6	0.9	0.09	8	0.022	2
(d)	88	6	0.9	0.18	10		
(e)	245	6	2.5	0.15	5	0.060	2
(f)	245	6	2.5	0.42	10		

III. PIXEL OPERATION, EXPERIMENTAL SETUP, AND MEASUREMENTS

An AM-OLED pixel circuit contains at least two TFTs with one storage capacitor $C_{\rm ST}$ [9]; when the switching TFT (SW TFT) is turned on during the programming state, the data signal voltage is stored at the storage capacitor through the switching TFT. Then, when the switching TFT is turned off during the driving state, the stored data voltage in $C_{\rm ST}$ will generate the node voltage V_S at the gate electrode of the driving TFT (DR TFT), which will maintain the constant OLED current flow through the driving TFT, and light emission from the OLED will occur, as expressed in the following equation and in Fig. 3:

$$I_{\rm OLED} = \beta(V_S - V_{\rm TH})^2, \text{ where } \beta = C_{\rm OX}\mu_{\rm FE}W_{\rm DR}/2L_{\rm DR}. \quad (1)$$

Here, $C_{\rm OX}$ is the gate insulator capacitance, $\mu_{\rm FE}$ is the field-effect mobility, $W_{\rm DR}$ is the channel width, and $L_{\rm DR}$ is the channel length of the driving TFT. Since the gate voltage of the DR TFT ($V_{\rm DD}$) is a dc bias high enough to make the DR TFT work in the saturation regime, the level and shape of the OLED current is solely determined by the gate voltage of the DR TFT (V_S) during operation, as shown in Fig. 3(b). Therefore, here, we fabricated different a-Si:H TFT structures with various storage and overlap capacitors, as shown in the blocked area in Fig. 3(a), to investigate the evolution of the gate voltage of the DR TFT (V_S) under various dynamic operational conditions. By investigating the variation of V_S, the behavior of $I_{\rm OLED}$ during the dynamic pixel circuit operation can directly be estimated from (1) for the given device electrical parameters.

The experimental setup used for measuring the dynamic characteristics of the a-Si:H TFT with a storage capacitor is as follows: HP8114A and HP8110A pulse generators are connected to the gate and drain electrodes for applying gate and drain signals, respectively. An active probe by GGB Industries, Inc. (Picoprobe 18B model), is used to measure the voltage variation stored at the storage capacitor by the probing source electrode. Since the picoprobe has a very low input capacitance of 0.02 pF and a very high input impedance (input leakage of 10 fA) compared with the a-Si:H TFT with a storage capacitor, it nominally has no perturbing effect on the whole circuit. An HP54615B digital oscilloscope with a bandwidth of 500 MHz was used to monitor the waveform change during the dynamic operation. A program based on National Instruments' LabVIEW virtual instrument commands was used to retrieve the scanned waveform from the oscilloscope. All measurements were done at room temperature in a dark box.

IV. EXPERIMENTAL RESULTS

In the dynamic pixel operation, two main properties of transistor are important, namely, the pixel charging performance and the feedthrough voltage. The charging time of the pixel circuit (i.e., the time required to charge up the storage capacitor in the pixel electrode circuit to the programmed level) determines the switching speed of the switching TFT and the programming speed of the driving TFT. Insufficient charging of the pixel electrode circuit can cause an error in either the OLED brightness or the display grayscale resolution as in the AM-LCDs [10]. The TFT charging performance is particularly important for high-resolution displays, where the available pulsewidth for the gate signal is relatively short in comparison to the low-resolution displays. Therefore, it is necessary for TFTs to have proper electrical characteristics such as high mobility and ON-current, which allow one to fully charge up the pixel circuits within the fixed pulsewidth or frame time. It should be noted that in the real display, two charging steps occur at the same time for charging the data voltage to the gate node of the driving TFT in the pixel: 1) data line charging from the driver IC to the drain node of the switching TFT involving the cross area of the data line and the scan line and 2) pixel charging from the data line to the gate node of the driving TFT. In this paper, the charging characterization within the single pixel circuit for the second case is mainly discussed.

The feedthrough voltage is another major issue in a-Si:H TFT AM-OLEDs. As aforementioned, during AM-OLED pixel

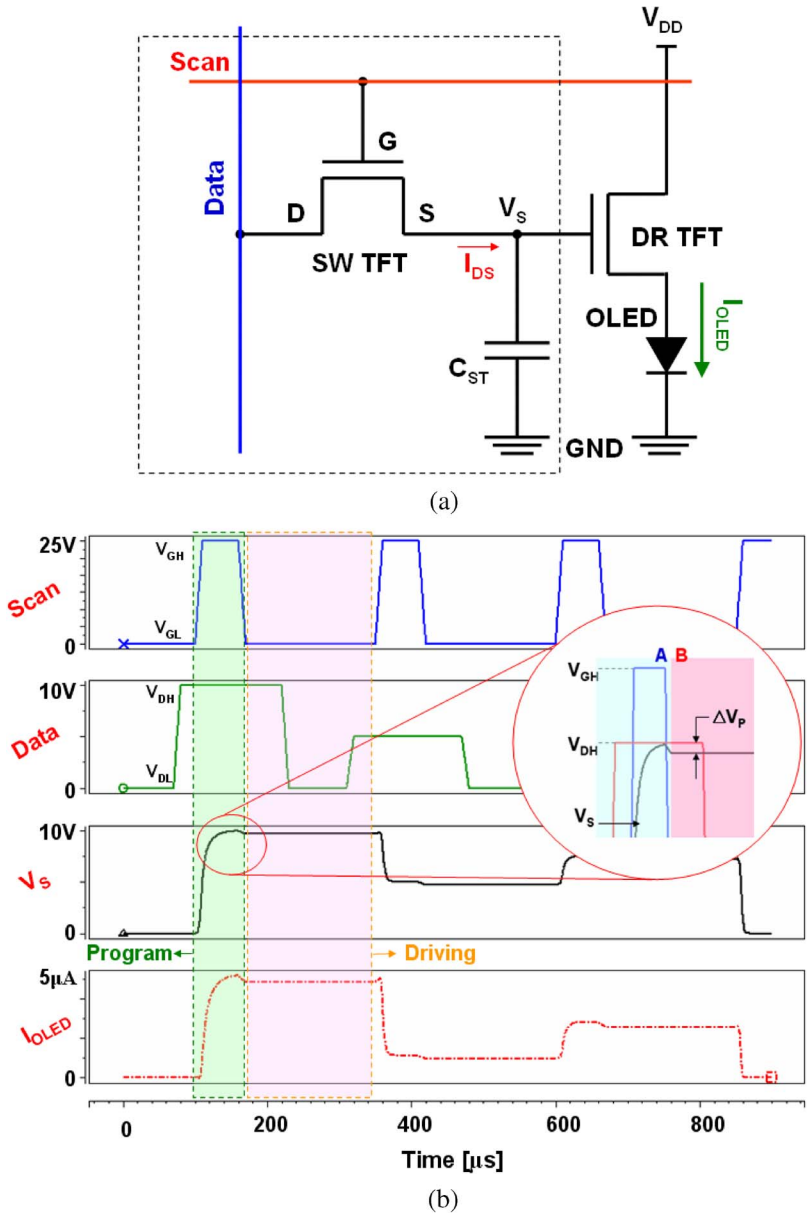

Fig. 3. (a) Schematic of a conventional AM-OLED pixel electrode circuit with two transistors and a storage capacitor [8]. (b) Operational driving signal waveforms simulated by HSPICE during programming and driving states. A and B represent the time right before and after the falling edge of gate pulse, respectively.

circuit operation, the potential at the gate node of the driving TFT V_S is supposed to remain constant and should be maintained at this value by the storage capacitor connected to the gate node during the driving state. This will provide an exact programmed OLED current during the pixel driving stage. However, due to the switching TFT dynamic operation, the gate node of the driving TFT suffers a potential variation, the so-called feedthrough voltage, due to the parasitic capacitor of the switching TFT [Fig. 3(b)]. The presence of the feedthrough voltage induces the dc offset voltage across the driving TFT and influences the amplitude of the OLED current flowing through the driving TFT. This voltage variation can be estimated in the actual pixel circuit design by considering the geometrical and electrical parameters such as the size of the storage capacitor, the size of the overlap capacitor between the gate and the source, and the amplitude of the switching TFT gate signal. A detailed discussion on the feedthrough voltage will be presented in the following section.

Fig. 3(b) shows an example of operational waveforms of the input signals $V_{\rm GS}$ and $V_{\rm DS}$ and the pixel voltage variation V_S measured at the storage capacitor, where $V_{\rm GH}$ and $V_{\rm GL}$ are the high and low levels of gate voltage, respectively, and $V_{\rm DH}$ is the high level of drain voltage. First, the data voltage pulse (Data) is applied to the drain electrode of the SW TFT. When the gate voltage pulse is applied to the gate electrode of the SW TFT, the SW TFT is turned on, and the storage capacitor is charged up to the data voltage during the one scan line time. When the gate pulse is removed, the data (or pixel) voltage is stored at the storage capacitor until the next gate and data signals are applied to reset the storage capacitor with a new data voltage for the next frame time. It should be noted that there is a voltage drop occurring at the falling edge of the gate signal (A). This voltage

TABLE II
EXAMPLES OF THE DRIVING VOLTAGE LEVELS USED IN THE EXPERIMENTAL SETUP

V_{GH}	V_{GL}	V_{DH}	$t_{G\text{-}ON}$	$t_{D\text{-}ON}$
25V	-5V	10V	40 µs	100 µs

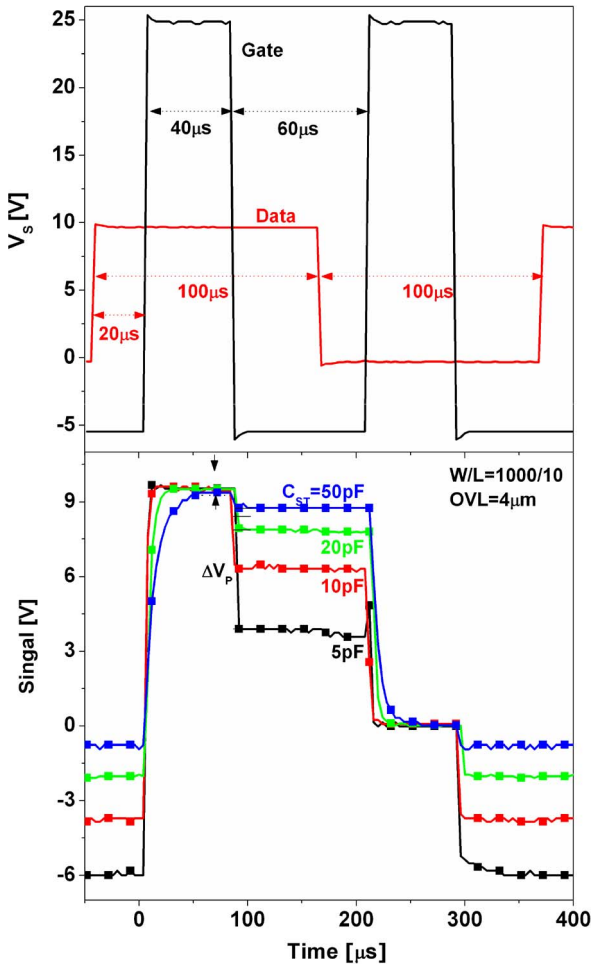

Fig. 4. Evolution of the measured pixel electrode voltage with the charging time for top-gate a-Si:H TFTs with different storage capacitors and corresponding operational gate and drain signal waveforms.

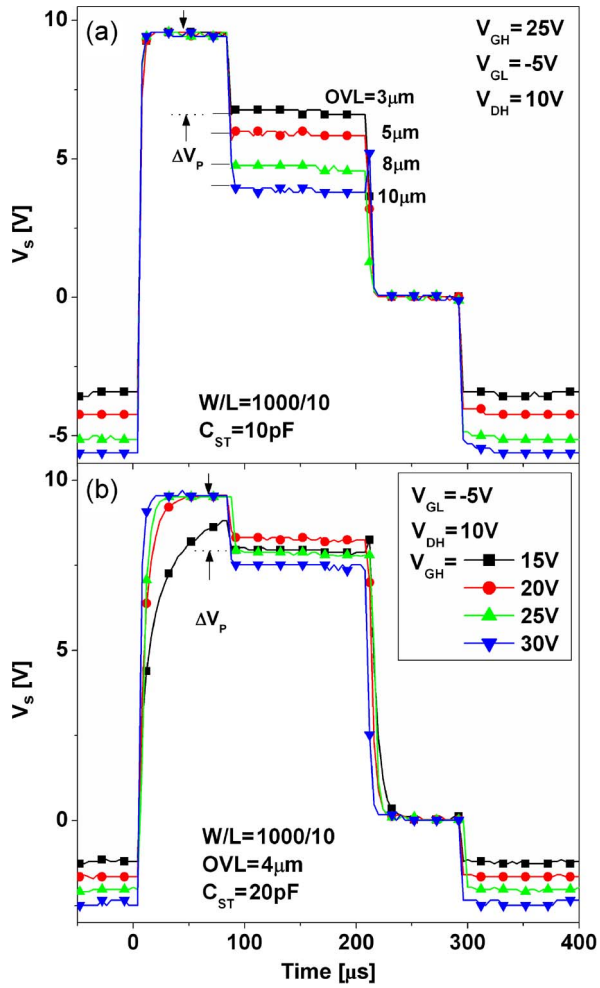

Fig. 5. Evolution of the measured pixel electrode voltage with the charging time for top-gate a-Si:H TFTs with (a) different gate-to-source overlaps and (b) different gate voltage levels.

drop ΔV_P is caused by the parasitic capacitance of the a-Si:H TFT associated with the gate-to-source capacitance $C_{\rm GS}$ due to the electrode overlap, which will be discussed in detail in the next section.

Here, we mainly focus on the influence of the variation of the storage capacitor and signal driving scheme on the charging characteristics of the top-gate a-Si:H TFT, whereas other parameters are kept at the same values ($W = 1000$ μm and $L = 10$ μm), and the extracted field-effect mobility and threshold voltage are 0.25 $\rm cm^2/V \cdot s$ and 6.9 V, respectively. Table II shows the driving voltage levels used in the notation in Fig. 3(b). The driving voltage levels were selected for typical AM-OLED driving signals. Gate and drain pulsewidths are selected as 40 and 100 μs, respectively, to assure sufficient charging time for different experimental conditions. Fig. 4 shows the pixel voltage V_S as a function of charging time for different storage capacitors. As shown in the figure, for fixed TFT geometry and driving signal conditions, the pixel charging time is proportional to the storage capacitance value, whereas ΔV_P becomes smaller when $C_{\rm ST}$ becomes larger. We will discuss the ΔV_P behavior in more detail in the following section.

In the a-Si:H TFT structural design, an important geometrical factor is the gate-to-S/D overlap (OVL). A narrow OVL could induce a current crowding effect at the S/D contacts, which effectively increases the series resistances and reduces the driving capability of the a-Si:H TFTs [11], [12]. On the other hand, a large OVL introduces a larger electrode overlap capacitance (parasitic capacitance), which is detrimental to display operation [13]. In addition, a larger OVL occupies a lager pixel area and reduces the overall pixel aperture ratio, which is not desirable particularly for high-resolution displays. Therefore, it is necessary to optimize the TFT electrode overlap in the a-Si:H TFT design. Fig. 5(a) shows the pixel charging characteristics of top-gate a-Si:H TFTs with different OVL values of 3, 5, 8, and 10 μm for a fixed $C_{\rm ST} = 10$ pF. The experimental results indicate that these a-Si:H TFTs nominally have the same switching and driving capabilities, whereas ΔV_P is proportional to OVL values. Fig. 5(b) shows the pixel voltage as a function of charging time for different high gate voltages

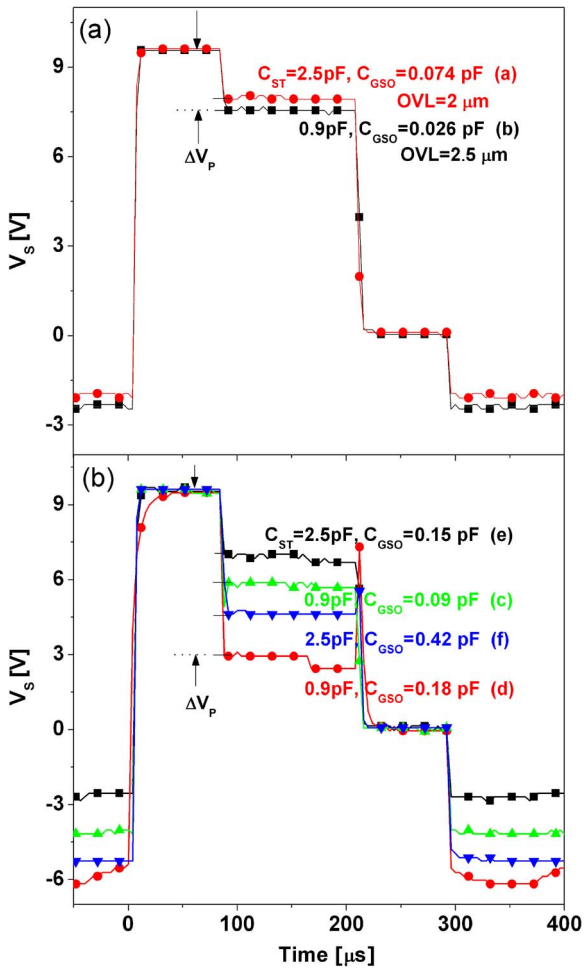

Fig. 6. Measured pixel electrode voltage for (a) normal and (b) Corbino a-Si:H TFTs with different storage and overlap capacitances. The detailed device geometry is given in Table I.

for $V_{\rm GL} = -5$ V. As $V_{\rm GH}$ increases from 20 to 30 V, the charging time decreases from 7.2 to 2.9 μs.

Based on the aforementioned experimental data and observation made for the top-gate a-Si:H TFT with different TFT geometries, we also measured the dynamic response of the bottom-gate Corbino a-Si:H TFT. To measure the feedthrough voltage of Corbino and normal a-Si:H TFTs, the same operational waveforms are used. Fig. 6(b) shows the measured pixel voltage for Corbino a-Si:H TFTs with different storage capacitances and overlap capacitances. The overlap capacitance $C_{\rm GSO}$ is calculated from the gate-to-source electrode overlap area and the gate insulator capacitance C_i, which is calculated as 15 nF/cm^2 by considering the dielectric constant ($\sim$6.8) and thickness ($\sim$4000 Å) of a-SiN$_x$:H. As shown in Fig. 6, as the overlap capacitance increases, the feedthrough voltage of the Corbino a-Si:H TFT increases for a fixed storage capacitor. At the same time, a larger storage capacitor induces a smaller feedthrough voltage in the Corbino a-Si:H TFT. A similar observation was made for the previously described top-gate a-Si:H TFTs. Fig. 6(a) shows the pixel voltage variation for a rectangular a-Si:H TFT with different storage and overlap capacitors. As shown in the figure, although the overlap capacitance is larger, if the storage capacitor is large enough, the feedthrough voltage can decrease. It should noted that all measurements for charging and feedthrough voltage characteristics of top- and bottom-gate a-Si:H TFTs used the same operational gate and drain waveforms, as shown in Fig. 4.

V. Discussions

A. Charging Characteristics of the a-Si:H TFTs

From Fig. 3(a), the charging of the storage capacitor can be expressed as

$$C_{\rm ST}\frac{d}{dt}(V_S - {\rm GND}) = I_{\rm DS} \tag{2}$$

where V_S is the gate voltage of the DR TFT, GND is the ground, and $I_{\rm DS}$ is the drain current flowing through the SW TFT. Assuming a gradual channel approximation, the $I_{\rm DS}$ in linear region operation can be described as

$$I_{\rm DS} = \mu_{\rm FE}C_i\frac{W}{L}(V_{\rm GH} - V_S - V_{\rm TH})(V_{\rm DH} - V_S) \tag{3}$$

where $(V_{\rm DH} - V_S) < (V_{\rm GH} - V_S - V_{\rm TH})$. Here, $\mu_{\rm FE}$ is the field-effect mobility, C_i is the gate insulator capacitance, W is the channel width, and L is the channel length. Combining (2) and (3), we can solve the differential equation and obtain the relation between the charging time $t_{\rm CH}$ and the pixel electrode voltage V_S, i.e.,

$$t_{\rm CH} = \frac{C_{\rm ST}\cdot L}{\mu_{\rm FE}C_iW}\cdot\frac{1}{(V_{\rm GH} - V_{\rm DH} - V_S)} \cdot\ln\frac{(V_{\rm GH} - V_S - V_{\rm TH})(V_{\rm DH} - {\rm GND})}{(V_{\rm GH} - V_{\rm TH} - {\rm GND})(V_{\rm DH} - V_S)}. \tag{4}$$

Equation (4) indicates that the pixel charging characteristics can be determined by the following factors: the storage capacitance $C_{\rm ST}$; the TFT geometries W, L, and C_i; the TFT electrical characteristics $\mu_{\rm FE}$ and $V_{\rm TH}$; and the signal driving schemes $V_{\rm GH}$ and $V_{\rm DH}$. Therefore, for a fixed pixel design and signal driving scheme, the charging characteristics depend on the a-Si:H TFT electrical characteristics; a longer charging time will result for TFTs with a higher threshold voltage at a given $\mu_{\rm FE}$ and a lower field-effect mobility at a given $V_{\rm TH}$.

Fig. 7 shows the charging time variation for different storage capacitor values extracted from Fig. 4. Here, the charging time is defined as the time required to charge the storage capacitor up to 90% of the drain signal level $(= 0.9 \times t_{\rm CH})$. We can conclude that the pixel electrode will be charged up much faster when the storage capacitor value is reduced to its minimum acceptable level. We fitted the variation of $t_{\rm CH}$ with $C_{\rm ST}$ using (4), shown as the solid line in Fig. 7, which shows an acceptable agreement with the measured data. The parameters used for this fitting are described in the figure. However, to get precise pixel charging characteristics of the AM-OLED, a more complete model will be required for both a-Si:H TFTs and OLED since the voltage dependence of the OLED was not taken into consideration in the aforementioned calculation.

Fig. 7 also shows the charging time $t_{\rm CH}$ variation for different gate voltage values $V_{\rm GH}$ and the fitted variation of $t_{\rm CH}$

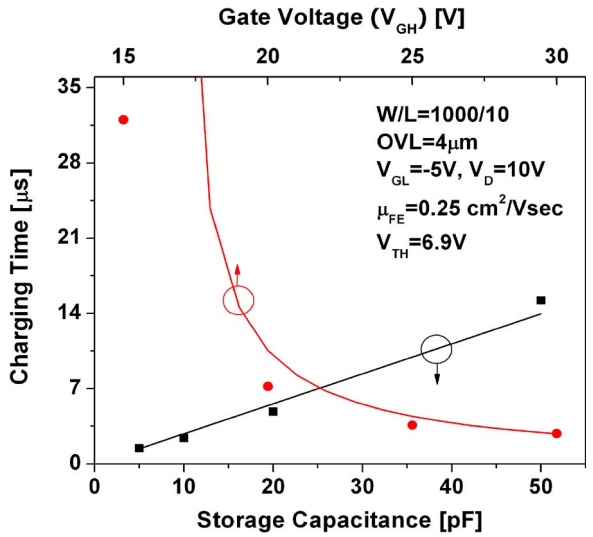

Fig. 7. Variation of the charging time as a function of the storage capacitor $C_{\rm ST}$ and the gate voltage $V_{\rm GH}$ for the top-gate a-Si:H TFT. (Symbols) Measured data. (Solid line) Calculated data using (4).

with $V_{\rm GH}$ using (4) (shown as the solid line). As shown in the figure, it should be noted that when the gate voltage is not high enough $(= 15\ {\rm V})$, the charging time becomes very long, so that the pixel electrode cannot be quickly charged up to the programmed voltage value $(= 10\ {\rm V})$, which deteriorates the display grayscale. Therefore, in pixel electrode operation, the gate voltage should be set high enough to minimize the charging time to reach the programmed value. However, at the same time, a high gate voltage induces high power consumption and a large pixel voltage variation ΔV_P when the gate voltage of the TFT is turned off. Therefore, the optimum gate voltage value should be considered in the AM-OLED pixel electrode design for a given resolution. It should be noted that the fitted curve in Fig. 7 shows an acceptable agreement with the measured data for the gate voltage range from 25 to 30 V. However, as the gate voltage decreases below 25 V, the operation of transistor starts to move from a linear to a cutoff regime. As a result, (4) becomes invalid and shows deviations from the measured values.

B. Feedthrough Voltage of the a-Si:H TFTs

The feedthrough voltage ΔV_P is the voltage drop of the gate node V_S of the driving TFT during the switching off of the gate signal of the switching TFT [Fig. 3(b)]. This voltage drop is mainly due to the existence of the SW TFT gate-to-source parasitic capacitance $C_{\rm GS}$, which causes the charge redistribution when the SW TFT is turned off by the gate signal. Fig. 3(a) shows the schematics of the a-Si:H TFT with a storage capacitor. In this circuit, the feedthrough voltage ΔV_P can be expressed as

$$\Delta V_P = \frac{C_{\rm GS}}{C_{\rm GS}+C_{\rm ST}}\Delta V_{\rm SCAN},\ \text{where}\ \Delta V_{\rm SCAN} = V_{\rm GH} - V_{\rm GL}. \tag{5}$$

It should be noted that the parasitic capacitors of the DR TFT do not have influence on the feedthrough voltage or gate potential

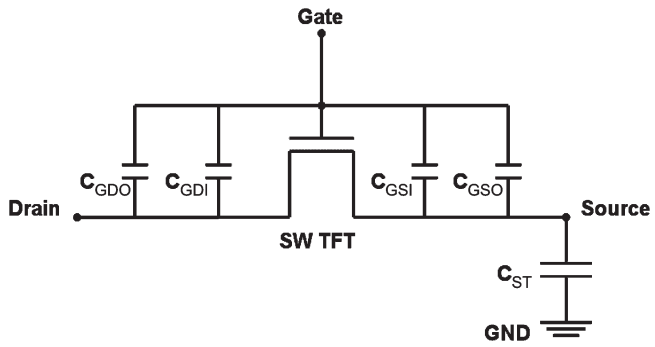

Fig. 8. Equivalent circuit of the a-Si:H TFT with the gate-to-S/D parasitic capacitances.

of the DR TFT since they are connected to constant dc bias components, i.e., $V_{\rm DD}$ and GND.

The derivation of (5) is based on the assumption that $C_{\rm GS}$ is independent of gate bias. However, in reality, $C_{\rm GS}$ is a metal–insulator–semiconductor (MIS) capacitor, which is known to be gate voltage dependent. Therefore, to obtain the accurate feedthrough voltage for the a-Si:H TFT, the gate voltage dependence of $C_{\rm GS}$ should be taken into consideration. The total gate-to-source capacitance $C_{\rm GS}$ can approximately be divided into the gate-to-source overlap capacitance $C_{\rm GSO}$ and the gate-to-source MIS intrinsic capacitance $C_{\rm GSI}$. Thus

$$C_{\rm GS} = C_{\rm GSO} + C_{\rm GSI}. \tag{6}$$

The equivalent circuit for the TFT parasitic capacitances is shown in Fig. 8, and the overlap capacitance can be expressed as the sum of two areal capacitances in series in the overlap area, i.e.,

$$\begin{aligned} C_{\rm GSO}\ (F\cdot m^2) &= W\cdot {\rm OVL}\cdot (C_i \| C_{\rm Si}) \\ &= W\cdot {\rm OVL}\cdot \frac{C_i C_{\rm Si}}{C_i + C_{\rm Si}} \end{aligned} \tag{7}$$

where W is the TFT channel width, C_i is the gate insulator areal capacitance (in farads), and $C_{\rm Si}$ is the a-Si:H areal capacitance (in farads). The gate-to-source MIS capacitance $C_{\rm GSI}$ is only valid when the TFT is in the ON-state. When the switching TFT changes from ON- to OFF-state, the channel charge injection occurs through $C_{\rm GSI}$, which causes the pixel voltage drop stored in the storage capacitor [14]. On the other hand, when the TFT is in the OFF-state, the a-Si:H layer behaves as an insulator, and there is no intrinsic parasitic capacitance. Thus

$$C_{\rm GSI} = 0, \qquad \text{for}\ V_G - V_S < V_T. \tag{8}$$

From the aforementioned analysis, we can express $C_{\rm GS}$ for the ON- and OFF-states as

$$\begin{aligned} C_{\rm GS-ON} &= C_{\rm GSO} + C_{\rm GSI} \\ &= W\cdot {\rm OVL}\cdot \frac{C_i C_{\rm Si}}{C_i + C_{\rm Si}} + C_{\rm GSI}, \qquad \text{for}\ V_G - V_S > V_T \end{aligned} \tag{9}$$

$$\begin{aligned} C_{\rm GS-OFF} &= C_{\rm GSO} \\ &= W\cdot {\rm OVL}\cdot \frac{C_i C_{\rm Si}}{C_i + C_{\rm Si}}, \qquad \text{for}\ V_G - V_S < V_T. \end{aligned} \tag{10}$$

To derive a more accurate expression for the feedthrough voltage, we can use the waveforms shown in Fig. 3(b) and the ON- and OFF-state gate-to-source capacitance. The charge stored at the source electrode right before (A) and after (B) the falling edge of the gate pulse, respectively, can be expressed as

$$Q_A = C_{\mathrm{GS-ON}}(V_{\mathrm{DH}} - V_{\mathrm{GH}}) + C_{\mathrm{ST}}(V_{\mathrm{DH}} - \mathrm{GND})$$
$$Q_B = C_{\mathrm{GS-OFF}}(V_S - V_{\mathrm{GL}}) + C_{\mathrm{ST}}(V_S - \mathrm{GND}). \quad (11)$$

According to charge conservation, since $Q_A = Q_B$, we then have

$$C_{\mathrm{GS-ON}} \cdot V_{\mathrm{DH}} - C_{\mathrm{GS-ON}} \cdot V_{\mathrm{GH}} + C_{\mathrm{ST}} \cdot V_{\mathrm{DH}} - C_{\mathrm{ST}} \cdot \mathrm{GND} = C_{\mathrm{GS-OFF}} V_S - C_{\mathrm{GS-OFF}} \cdot V_{\mathrm{GL}} + C_{\mathrm{ST}} \cdot V_S - C_{\mathrm{ST}} \cdot \mathrm{GND}. \quad (12)$$

If we add the $C_{\mathrm{GS-OFF}} \cdot V_{\mathrm{DH}}$ term on both sides and organize the equation

$$\therefore\ |\Delta V_P| = \frac{C_{\mathrm{GS-OFF}}}{C_{\mathrm{GS-OFF}} + C_{\mathrm{ST}}} \Delta V_G + \frac{C_{\mathrm{GS-ON}} - C_{\mathrm{GS-OFF}}}{C_{\mathrm{GS-OFF}} + C_{\mathrm{ST}}} (V_{\mathrm{GH}} - V_{\mathrm{DH}}). \quad (13)$$

If we assume that $m = C_{\mathrm{GS-ON}}/C_{\mathrm{GS-OFF}}$, the equation becomes

$$\therefore\ |\Delta V_P| = \frac{C_{\mathrm{GS-OFF}}}{C_{\mathrm{GS-OFF}} + C_{\mathrm{ST}}} \left[\Delta V_G + (m-1)(V_{\mathrm{GH}} - V_{\mathrm{DH}})\right]. \quad (14)$$

Equation (14) will be used to verify the experimental data obtained for the staggered a-Si:H TFTs. It should noted that if $C_{\mathrm{GS-ON}} = C_{\mathrm{GS-OFF}}$, the equation is reduced to (5).

Fig. 5 shows the measured pixel voltage for top-gate a-Si:H TFTs with different gate-to-source overlaps. The figure clearly shows that the feedthrough voltage increases with the increasing gate-to-source overlap widths, and it indicates that an optimum overlap need be defined to minimize the feedthrough voltage. However, at the same time, the OVL should not degrade the a-Si:H TFT pixel charging performance. The pixel electrode voltage variation for different gate voltage levels is also shown in Fig. 5. As the gate voltage increases from 15 to 30 V, the feedthrough voltage becomes larger from 0.9 to 2.2 V, as predicted by (14). Therefore, the optimization of the driving signal should be done based on the consideration of the feedthrough voltage effect on the display operating performance.

Fig. 4 shows the measured pixel voltage for a-Si:H TFTs with different storage capacitances. All a-Si:H TFTs have a channel width of 1000 μm, a channel length of 10 μm, and a gate-to-S/D overlap of 4 μm. As shown in the figure, the feedthrough voltage increases with the decreasing storage capacitance value.

Fig. 9 shows the variation of the feedthrough voltage as a function of the ratio $C_{\mathrm{GSO}}/(C_{\mathrm{ST}} + C_{\mathrm{GSO}})$. Considering the dielectric constant (~6.8) and thickness (~3300 Å) of a-SiN$_x$:H, the OFF-state gate-to-source capacitance $C_{\mathrm{GS-OFF}} = C_{\mathrm{GSO}} =$ 0.73 pF for the top-gate a-Si:H TFT. By fitting the experimental data with (14), we obtained the fitting parameter $m =$ 2.5. It indicates that the ON-state total gate-to-source capacitance $C_{\mathrm{GS-ON}} = m \times C_{\mathrm{GS-OFF}} = 2.5 \times C_{\mathrm{GS-OFF}}$. As in

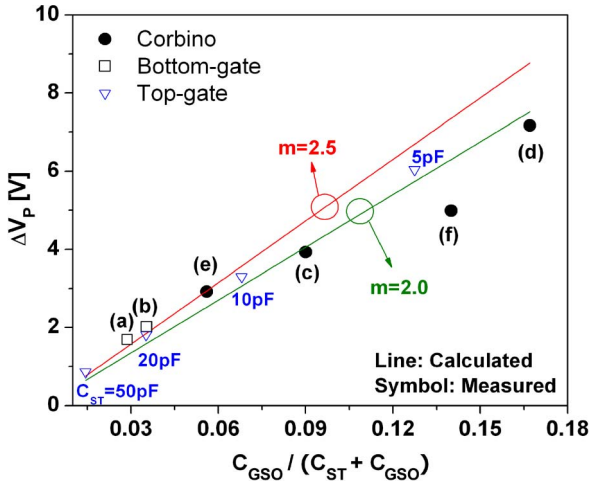

Fig. 9. Feedthrough voltage ΔV_P variation for Corbino a-Si:H TFTs as a function of the ratio $C_{\mathrm{GSO}}/(C_{\mathrm{ST}} + C_{\mathrm{GSO}})$. (Closed symbols) Measured values for Corbino a-Si:H TFTs. (Open symbols) Measured values for rectangular top- and bottom-gate a-Si:H TFTs. (Solid lines) Calculated values using (14) with the fitting parameter $m = 2.5$ and 2.0. (a)–(d) Different Corbino a-Si:H TFTs and (e)–(f) rectangular bottom-gate a-Si:H TFTs that are summarized in Table II.

(9), since $C_{\mathrm{GS-ON}}$ consists of the gate-to-source overlap capacitance and intrinsic gate-to-source MIS capacitance, the C_{GSI} for the ON-state is about $1.5 \times C_{\mathrm{GSO}}$, which is about half of the total channel intrinsic capacitance $W \times L \times C_i$ ($\approx$ 1.8 pF). This result suggests that for the top-gate a-Si:H TFTs, the ON-state gate-to-drain MIS intrinsic capacitance C_{GDI} is also about half of the total channel intrinsic capacitance. This result for the top-gate a-Si:H TFT shows a good agreement with the intrinsic capacitance model reported for crystalline MOSFETs, which predicts that when a MOSFET is in the linear ON-state, the gate-to-S/D capacitance is about half of the total channel capacitance [15]. Fig. 9 also shows the variation of the measured feedthrough voltage of rectangular top- and bottom-gate a-Si:H TFTs and Corbino a-Si:H TFTs as a function of the ratio $C_{\mathrm{GSO}}/(C_{\mathrm{GSO}} + C_{\mathrm{ST}})$. From (14), the variation of the feedthrough voltage for different Corbino a-Si:H TFTs with different storage capacitor values was calculated based on the geometries and operational waveforms. As shown in figure, the calculated feedthrough voltages of the rectangular a-Si:H TFT using (14) show a good agreement with the measured values. This means that (14) is valid for both top- and bottom-gate a-Si:H TFT structures. However, different from rectangular a-Si:H TFTs, the calculated values for the Corbino a-Si:H TFT show some deviation from the measured values. This deviation can be associated with the unique geometry of the Corbino a-Si:H TFT. Considering the fitting parameter $m = C_{\mathrm{GS-ON}}/C_{\mathrm{GS-OFF}}$, due to a large overlap between gate and source electrodes in Corbino a-Si:H TFTs in comparison to a normal rectangular a-Si:H TFTs (Table I), an increase in $C_{\mathrm{GS-OFF}}$ ($= C_{\mathrm{GSO}}$) causes a decrease in the fitting parameter m. Consequently, when we change the fitting parameter for the Corbino a-Si:H TFT from 2.5 to 2.0 in (14), the correct calculated values show a good agreement with the measured feedthrough voltage values. However, it is observed that there is still a small deviation at a high $C_{\mathrm{GSO}}/(C_{\mathrm{GSO}} + C_{\mathrm{ST}})$ ratio, Therefore, a more thorough study is needed for the

Corbino a-Si:H TFT with different TFT geometries to find out the proper fitting parameter m in (14) to predict the feedthrough voltage variation, which is critical in programming the gate voltage for the driving TFT to express a large range of grayscale levels in the AM-OLED. In particular, for the a-Si:H TFTs with asymmetric shape of electrodes, (14) with the modified fitting parameter will be a good approximation to estimate the feedthrough voltage variation for designing the operational waveforms and the pixel electrode circuits for AM-OLEDs.

VI. Influence of Corbino a-Si:H TFTs on the OLED Current

As we have previously described, the dynamic characteristics (charging performance and feedthrough voltage variations) of the a-Si:H TFT are closely related to the capacitive elements (the overlapped capacitor and the storage capacitor) and operational signals in the pixel electrode circuit. In general, as the display resolution of the AM-OLED becomes higher because the pixel area becomes smaller, the size of the storage capacitor is predetermined to be as small as possible to achieve the highest possible pixel aperture ratio. The overlapped capacitance is usually predetermined by the TFT processing design rules and can hardly be changed for a standard rectangular a-Si:H TFT. Operational signal waves are also predetermined depending on the pixel driving circuitry to minimize power consumption for a given AM-OLED grayscale range. Therefore, for a given AM-OLED pixel circuit with standard rectangular a-Si:H TFTs, all these parameters are fixed to the designed values and cannot be changed to reduce the charging time or feedthrough voltage.

However, as the AM-OLED pixel circuit becomes complicated with the compensation functions [16], [17], the control of the feedthrough voltage becomes more necessary since it directly impacts the OLED current levels during the driving state of the AM-OLED. From Fig. 3, the OLED current during the programming state can be expressed by (1). If we assume the feedthrough voltage given by (14), the OLED current during the driving state (after the switching TFT is turned off) is expressed as

$$\begin{aligned} I_{\mathrm{OLED}} &= \beta(V_S - V_{\mathrm{TH}} - \Delta V_P)^2 \\ &= \beta\left(V_S - V_{\mathrm{TH}} - \frac{C_{\mathrm{GSO}}}{C_{\mathrm{GSO}} + C_{\mathrm{ST}}} \right. \\ &\qquad \left. \times [\Delta V_G + (m-1)(V_{\mathrm{GH}} - V_{\mathrm{DH}})]\right)^2. \end{aligned} \quad (15)$$

Therefore, for the given pixel circuit design and operational conditions, the variation of the OLED current between programming and driving states can be suppressed by minimizing the overlap capacitance of the switching TFT, which results in a minimized feedthrough voltage. Due to a unique geometry of the Corbino a-Si:H TFT, the size of the source electrode can be minimized in comparison to the drain electrode, whereas the channel width is maintained to the designed value. Therefore, the overlapped area between source and gate electrodes is minimized, resulting in a minimized overlapped gate-to-source capacitance C_{GSO} in comparison to the rectangular TFT with the same channel width. Hence, a relatively much smaller

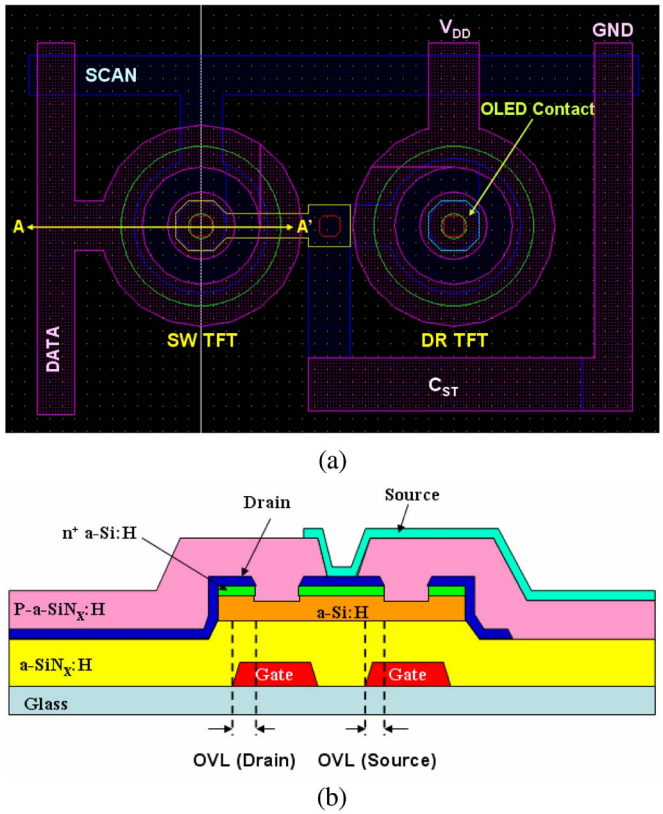

Fig. 10. (a) Layout of the pixel electrode circuit in Fig. 3 with Corbino a-Si:H TFTs as switching and driving TFTs. (b) Cross-sectional view of the Corbino a-Si:H with a patterned gate electrode.

feedthrough voltage is expected to be achieved for the Corbino a-Si:H TFT [7] if used as a switching TFT in AM-OLEDs. It should be noted that in AM-OLED operation, the polarity of the data signal voltage (gate node of the DR TFT) is always positive to make sure that the OLED current is flowing all the time. Therefore, in the AM-OLED, the positions of the drain and source electrodes of the Corbino TFT can be fixed so that a unique asymmetric geometry does not affect the OFF-current behavior of the Corbino a-Si:H TFT [7], which would be influenced by a line- or a dot-inversion method, resulting in a Mura defect in the AM-LCD [18]. In addition, in the Corbino a-Si:H TFT, C_{GSO} can further be reduced by patterning the gate electrode. As shown in Fig. 10, the gate electrode can be patterned to minimize the overlapped area with the source electrode, which can further reduce the feedthrough voltage for a given AM-OLED pixel circuit design. As shown in Table I for target values, when the overlap area is reduced to 2 μm, the corresponding values of C_{GSO} in Corbino TFTs further decrease in comparison to the normal TFTs with the same channel width. In this specific case, it is calculated that there are 16.2% and 19.4% decreases for the channel widths of 88 and 245 μm, respectively. Therefore, by using the Corbino a-Si:H TFT in AM-OLEDs, we can expect a better control of the OLED current grayscale levels, as well as better electrical stabilities [7]. Fig. 10 shows an example of the layout of pixel electrode circuits for the AM-OLED with the Corbino a-Si:H TFTs as switching and driving transistors. It should be noted that when a large channel width is required for the driving TFT

to achieve a large drain current level for the same gate voltage, the multiple hexagonal a-Si:H TFT can alternatively be used to avoid the waste of the large pixel area to be occupied by the single Corbino a-Si:H TFT [19].

VII. Conclusion

In this paper, the dynamic characteristics of various a-Si:H TFTs have been discussed. The experimental results indicated that the charging performance of the a-Si:H TFT depends on the size of the storage capacitor connected to the source of the TFT and gate voltage level, but it is independent of the overlap capacitance. We have also measured the feedthrough voltage characteristics for various top- and bottom-gate a-Si:H TFTs with different device geometries. The feedthrough voltage was shown to be closely related to the value of the storage capacitance, the overlap capacitance, and the operational waveforms. Analytical expressions were derived to compare the calculated data with the experimental results, and a good agreement between the experimental and calculated results was obtained for all the studied a-Si:H TFTs. Due to a unique geometry, the Corbino a-Si:H TFT requires modification in the fitting parameter of the analytical equation. We believe that the derived analytical expressions represent a very useful tool in the design of the pixel electrode circuits and operational signals for AM-OLEDs. Using the Corbino a-Si:H TFT as a switching TFT in the AM-OLED pixel circuit, we can expect that the feedthrough voltage variation can be minimized to maintain the programmed OLED current levels.

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